Luyuan Ge

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Education

University of Toronto — Toronto, Canada
Bachelor of Science in Software Engineering — *Sep. 2023 – June 2027 (Expected)*

- **GPA**: 3.7/4.0 | **Relevant Coursework**: Computer Organization, Operating Systems, Algorithms, Software Design, Calculus, Linear Algebra, Computer Networks.

Experience

ByteDance — Beijing, China
Research Intern – Spatial Intelligence — *Sep. 2025 – Dec. 2025*

- Developed a **Vision-Language-Action (VLA)** model to enhance spatial reasoning by integrating 3D geometry with semantic understanding for robotics applications.
- Engineered a multimodal fusion pipeline: utilized **MapAnything** for 2D-to-3D reconstruction and combined spatial coordinates with **SigLIP** embeddings to feed the **LLaVA-3D** backbone.
- Designed a generative action head using **Flow Matching** to accept the VLM's high-dimensional output and generate precise continuous action tokens for downstream control tasks.

China Unicom — Beijing, China
Software Engineering Intern – AI Infrastructure — *May 2025 – Aug. 2025*

- Architected an autonomous agent system ingesting diverse unstructured (Images, Docs) and structured (Excel) data, routing to a hybrid **MongoDB**/**PostgreSQL** storage layer.
- Built a dynamic **RAG** engine on vectorized data, enabling natural language querying and real-time analytics generation (Charts, Excel reports) without manual intervention.
- Implemented the **Model Context Protocol (MCP)** to define modular agent skills for complex database operations (CRUD) and autonomous schema evolution.

Technical Skills

Languages: C, C++, Python, Rust (Basic), Go, MIPS/RISC-V Assembly, Verilog, Java
Systems & Low-Level: Linux Kernel Modules, GDB, Valgrind, Perf, Strace, QEMU, Makefile, CMake
Architecture & Hardware: gem5, Verilator, Vivado, FPGA Prototyping, CUDA, Cache/Pipeline Design
Infrastructure: Docker, Kubernetes, AWS (EC2/S3), Kafka, PostgreSQL, Redis, GitLab CI/CD, Nginx
AI/ML: PyTorch, Hugging Face, vLLM, Transformer Architecture, LoRA, LangChain, LangGraph

Projects

5-Stage Pipelined RISC-V Processor | *Verilog, Verilator, Vivado, RISC-V ISA*

- Designed and implemented a **5-stage pipelined RV32I processor** in Verilog, supporting 37 base integer instructions with full **data forwarding** and **hazard detection** logic.
- Verified functional correctness against the official **RISC-V test suite** using Verilator simulation, achieving 100% pass rate on all RV32I compliance tests.
- Synthesized the design targeting a Xilinx Artix-7 FPGA via **Vivado**, achieving **85 MHz** max clock frequency with 3,218 LUTs (15.5% utilization) and 2 BRAMs for register file and instruction memory.

Linux Kernel Character Device Driver | *C, Linux Kernel API, QEMU, GDB*

- Developed a loadable kernel module implementing a character device with **read/write/ioctl** interfaces and a kernel-space **ring buffer**, supporting concurrent access via **mutex** and **spinlock** synchronization primitives.
- Built a debug workflow using **QEMU** VMs with **KGDB** for kernel debugging and **ftrace/printk** for tracing execution paths through the driver's interrupt and I/O handling routines.

Bare-Metal MIPS Systems Programming | *MIPS Assembly, C, QEMU, Python*

- Built a bare-metal graphics application on **32-bit MIPS** emulated via QEMU, directly managing CPU registers, stack frames, and **memory-mapped I/O** without OS abstraction; implemented a custom **framebuffer rendering engine** writing directly to display memory addresses.
- Optimized critical Assembly loops via **branch delay slot utilization** and **register allocation** strategies to minimize pipeline stalls; engineered a real-time physics simulation (collision, gravity) entirely in Assembly.

Summary

Systems-oriented software engineer with strong interest in computer architecture, device drivers, and AI infrastructure. Experienced in low-level C/Assembly, kernel development, and processor design. Passionate about bridging silicon and software.